Heiko Joerg **Schick**

Chief Architect | Advanced Computing and Artificial Intelligence

linkedin.com/in/heikojoergschick http://www.schihei.de
+49-151-54682218 heiko.schick@huawei.com info@schihei.de
0000-0003-0570-0615 Munich, Bavaria, Germany German Citizen

As Chief Architect at Huawei Technologies, my proficiency in artificial intelligence, innovative computer architectures, and heterogeneous computing bolsters the company's technological advancements and global standing in future-oriented technologies. My 12-year tenure at IBM Germany R&D, where I held critical roles in advanced computing, has refined my skills and provided valuable insights.

I take immense pride in promoting an organizational culture that values trust, diversity, and openness, which have enhanced the rate of our technological advancements and positioned us as a lynchpin for talent development and collaboration. This commitment is the driving force behind my contributions to current technological progress.

Professional Experience

Present
January 2021

Chief Architect | HiSilicon Turing Department, Huawei Technologies, Germany

- Conceptualized and developed advanced computing and artificial intelligence roadmaps focused on critical technologies aimed at providing strategic direction for executive management and technical fellows. This initiative helped to align technological developments with organization goals and prime decision-making processes.
- Led a diverse research team of 12 individuals comprised of Huawei employees, students, doctoral candidates, and external staff members. This multi-skilled team synergized various strengths and experiences—fostering a dynamic collaborative environment.
- Enhanced the Arm and AI ecosystem in Europe, specialising in weather simulation, life sciences, and computer-aided engineering—leading to developing next-generation SoC and low-level software technologies.
- Conducted a comprehensive assessment of the effects of run-time variability of parallel workloads on multi-core CPUs. This analysis allowed for a deeper insight into system performance under various workloads, facilitating the optimization of multi-core CPU utilization for parallel processing tasks.
- In collaboration with ThinkParQ, we enabled the BeeGFS filesystem for Arm, which showcases our commitment to advancing Arm's ecosystem and improving storage solutions within distributed systems.
- Integrated HPC and AI technologies into a single unified platform.
- Led R&D into Graph Neural Network (GNN) models for Huawei's AI portfolio.
- Provided assistance to my team in developing a video restoration project using AI models. This initiative advanced our capabilities in machine learning and video processing technologies.
- Conducted R&D for AI SoCs SW/HW solutions, optimising algorithms' exteroceptive and proprioceptive perception for legged locomotion.
- Analysed and optimised the architecture for sparse linear algebra hardware and software.
- Researched advancements in sparse optimisation methods in scientific computing.
- Evaluated performance of sparse linear solver frameworks on ARM-based architectures.
- Led the development and implementation of SVE-enabled libraries and typical European HPC application benchmarks.
- Represented Huawei in standardisation and industry activities, including strategic EU-level programmes such as the European Technology Platform for HPC (ETP4HPC).
- Promoted technical academia engagement programmes and cooperative projects.
- Managed recruitment for the HiSilicon team's advanced computing roles, including candidate screening, interviews, job description refinements, and recruitment coordination.

During my tenure in this position, I orchestrated advancements in European Arm and AI ecosystems, consolidated HPC and AI technologies, optimized systems, amplified Huawei's industry presence, and spurred academic partnerships and recruitment efforts.

Artificial Intelligence | GNNs | Reinforcement Learning | Supercomputing | HPC | ARM | SVE

December 2020
January 2019

Chief Architect | HiSilicon Turing Department, Huawei Technologies, Germany

- Facilitated the application of HiSilicon solutions by activating Arm for HPC/Arm+AI ecosystem in partnership with other firms and collated requirements for upcoming server systems.
- Actively collaborated with the global HiSilicon R&D team to design efficient SoC architectures geared towards advanced computing and autonomous driving.
- Represented Huawei in standardisation initiatives and industry activities, notably contributing to EU-level strategic undertakings such as the European Technology Platform for HPC (ETP4HPC).
- Spearheaded academic engagement programmes and fostered cooperative projects in the technical sector.
- Oversaw recruitment processes for the HiSilicon advanced computing team, handling tasks such as candidate screening, interview facilitation, job description modification, and recruiter liaison.

In this role, I orchestrated significant advancements in the European Arm and AI ecosystems, seamlessly integrated HPC with AI technologies, optimized systems for efficient operations, amplified Huawei's presence in industry-wide activities, and spurred effective academic partnerships and recruitment efforts.

Artificial Intelligence | Supercomputing | HPC | ARM | Team Building

December 2018
January 2015

Chief Architect | Central Hardware Department, Huawei Technologies, Germany

- Directed and recruited a specialized team of over 7 professionals dedicated to computational (micro-architecture), interconnect, and memory technologies.
- Successfully conceived and administered a project charter for an advanced Arm-based computing prototype, which involved outlining the project scope, identifying key technologies, and setting major milestones.
- Played a crucial role in refining architectural elements and enhancements for Arm-based computer systems, primarily in the sectors of computation, memory system, storage, switching, and interconnect.
- Proactively identified and researched innovative key technologies that added significant value to Huawei's system strategies.
- Conceived and facilitated the architectural framework for in-memory processing technologies, specifically designed for use in Arm-based systems.
- Forged productive collaborations with three prominent research and data centres in Europe to evaluate Arm-based systems and carry out experimental hardware co-design.
- Established strategic partnerships concerning Horizon 2020 projects focused on advanced computing.
- Acted as the chief representative to the Cache Coherent Interconnect for Accelerators (CCIX) standard, which was executed effectively in HiSilicon Kunpeng 920 SoC.
- Formulated and defined high-impact libraries and performance tools for the Arm architecture. I was also instrumental in generating requirements and implementing performance optimization strategies.
- Contributed significantly to the formation of a dedicated team with a primary focus on autonomous driving.

ARM | Computer Architecture | HPC | In-Memory Processing | CCIX | ETP4HPC | Research Collaborations

December 2014
January 2014

Senior Engineer | Systems Optimisations Competency Center, IBM Research & Development, Germany

- Led the technical and performance team for the SAP HANA in-memory, column-oriented, relational database management system on the IBM POWER architecture.
- Ensured the performance results aligned with competitive hardware configurations.
- Provided support to meet the performance objective by leading POWER-specific code development and conducting a comprehensive performance evaluation.
- Analyzed the use of hardware resources, including memory bandwidth, threads, cores, and sockets, during rigorous scaling tests.
- Defined the scale-out and scale-up system architecture and executed corresponding performance measurements.
- Thoroughly investigated hot functions at the micro-architecture level.
- Enhanced vector code coverage in SAP HANA by 6%, leading to a performance improvement of 15%.

SAP HANA | In-memory Databases | IBM System p | POWER Architecture | SAP-H | Springer | BW-EML

December 2013 – July 2011

Senior Engineer | Blue Gene Active Storage, IBM Research & Development, Germany

- Led a proficient technical engineering team of over eight individuals, accountable for the development and delivery of the Blue Gene Active Storage (BGAS) architecture.
- Successfully contributed to the BGAS architecture, ensuring a balanced integration of solid-state storage, computation, and cost-scalable network.
- Utilized Blue Gene/Q as an effective tool for swift prototyping of active storage concepts.
- Executed proofs-of-concept on computing-in-storage for applications in neuroscience and middleware software packages, including GPFS and DB2.
- Oversaw the architecture and development of various software packages (including peripheral image, device driver, FPGA image and middleware frameworks) for a hybrid scalable solid-state storage device targeted at research explorations.
- Decomposed acceleration functions for application in both industrial and scientific scenarios.
- Took charge of the development of a software-based RDMA network interface controller.
- Coordinated research collaborations with three customers in Germany, Switzerland, and the United Kingdom.
- Mentored Bachelor's and Master's students, providing academic guidance and professional development support.

Blue Gene/Q | Active Storage | BGAS | Computing-in-storage | GPFS | DB2 | Solid-state-storage

June 2011 – April 2009

Senior Engineer | Blue Gene/Q, IBM Research & Development, Germany

- Spearheaded a global PCI Express verification and performance team for the Blue Gene/Q ASIC, managing to complete the project ahead of schedule and within the specified performance parameters.
- Led and executed the hardware bring-up of the PCI Express core of the Blue Gene/Q ASIC, ensuring smooth and efficient functionality.
- Formulated the verification and performance plan while providing regular status updates to the executive management and our clients.
- Developed proxy applications to simulate parallel file-system traffic tunnelled via InfiniBand over PCI Express.
- Created a cutting-edge hardware simulation environment to replicate the operation of the Blue Gene/Q ASIC in combination with PCI Express attached devices, covering physical, link, and transport layers.
- Implemented an automatic regression framework for I/O traffic on ASICs, enhancing overall system performance and reducing potential troubleshooting time.

Blue Gene/Q | PCI Express | InfiniBand | Parallel Filesystems | ASIC | Simulation

March 2009 – January 2008

Resident Engineer | Open Systems Development, IBM Research & Development, Germany

- Led the initiation of the QPACE project and coordinated a team of over 15 developers from various industrial and academic partners, ensuring effective collaboration and smooth functioning.
- Was responsible for the architecture and development of the firmware for the compute node of the QPACE project, thereby ensuring the project's technical efficiency.
- Formulated and executed the bring-up plan for the QPACE project, providing clear direction and maintaining project deliverables.

The QPACE supercomputer, a joint project between various academic institutions, IBM Research, and other industrial partners, was designed as an energy-efficient, scalable architecture for high-performance computing, primarily used for lattice QCD calculations, and was notably recognized as the most energy-efficient supercomputer in the world on the Green500 list in 2009 and 2010.

Supercomputer | Prototype | Research Project | Cell/B.E

December 2007
September 2006

Resident Engineer | Open Systems Development, IBM Research & Development, Germany

- Made significant contributions to the firmware development of blade servers utilizing the PowerPC 970 and Cell/B.E. processor, enabling enhanced system performance.
- Took responsibility for the PCI Express device discovery algorithm, ensuring its efficient functioning and reliability.
- Ensured the hardware bring-up, compatibility, and performance of PCI Express-based InfiniBand adapters, optimizing overall system efficiency.
- Held accountability for the PCI Express compliance testing, with a focus on the physical layer, configuration space, link & transport layer, and platform configuration.
- Successfully led the AbiCell and NICOLL projects, showcasing leadership skills and achieving the predetermined objectives.

Linux | Firmware | PCI Express | InfiniBand | Cell/B.E. | PowerPC 970

August 2006
September 2004

Staff Engineer | I/O Firmware Development, IBM Research & Development, Germany

- Developed the Linux kernel framework and interrupt processing routines for the IBM System p InfiniBand and Ethernet device driver, ensuring smoother operation and enhanced performance.
- Ensured compatibility and performance in accordance with upper-level protocols such as the Message Passing Interface (MPI) standard, Socket Direct Protocol (SDP), and communications using TCP/IP over InfiniBand.
- Took the lead in coordinating the open-source and release process with the Linux kernel development community and Linux distributors, ensuring efficient dissemination and adoption.
- Directed the technical bring-up and development of a parallel cluster based on the PowerPC 970 processors and ultra-low latency InfiniBand network components.
- Contributed significantly to software optimizations and performance tests, leading QPACE to be recognized as one of the most energy-efficient supercomputers in June 2010.

Linux | Linux Kernel | Network | InfiniBand | Ethernet | IBM System p

August 2004
Mai 2004

Diploma Thesis | Processor Firmware Development, IBM Research & Development, Germany

Concept, Design and Implementation of a Slimline Boot Firmware for Linux on Power Architecture.

- Successfully defined, implemented, and demonstrated a technology innovation involving the packaging of binary program code within the firmware. This process allowed for later execution by the operating system using a compact virtual machine, terming a significant improvement in system operations.

Research Concept | Firmware | Operating System | Virtual Machine

April 2004
January 2003

Internship | Processor Firmware Development, IBM Research & Development, Germany

- Developed a Linux program aimed to trace program execution of machine instructions, improving transparency and debugging capabilities.
- Conducted detailed analysis of how machine instructions would execute in multiple processor pipelines of IBM mainframes, enhancing overall system understanding and performance.

Linux | Assembler | C | Processor Pipelines | IBM System z

October 2002
July 2002

Student Employee | Linux on System z Evaluation, IBM Research & Development, Germany

- Formulated and executed a comprehensive test plan for running over 100 Linux instances within a virtual machine environment on IBM mainframes, significantly enhancing system utilization.
- Carried out a performance assessment of the benefits of resource-sharing in overcommitment scenarios and during high-speed network communications, thereby optimizing system efficiency.

Linux | Virtual Machines | IBM System z | z/VM

February 2002
August 2001

Internship | Linux on System z Evaluation, IBM Research & Development, Germany

- Formulated and implemented a detailed test plan for a cryptographic Linux device driver for IBM mainframes, ensuring its security and functionality.
- Authenticated task offloading to installed cryptographic co-processors and acceleration devices, enhancing system performance and efficiency.
- Constructed an automatic testing framework for the execution of all verification tasks, ensuring thorough and consistent testing procedures.

Linux | Linux Kernel | Device Driver | Perl | IBM System z

Education

August 2004 – October 2000 | **Communication and Software Engineering, Albstadt-Sigmaringen University, Germany**
Final Grade: 1.2

Operating Systems | Computer Architecture | Communication Networks | Software Architecture

Outreach and volunteering

2019 **CODES@OEHI Hackathon**, Two-day hands-on workshop for current or prospective users of Arm-based HPC system to port their applications to such system or to further optimise already ported applications.

March 2010 – February 2010 | **Technical Consultant, IBM Research & Development, Philippines**
Volunteer Experience for IBM Corporate Service Corps, Disaster and Humanitarian Relief

- Advised the National Institute of Geological Sciences (NIGS) on creating real-time, interactive flood maps of Metro Manila, demonstrating expertise in data visualization.
- Consulted on the design and developed a benchmark system for a flood prediction platform, demonstrating cutting-edge expertise in environmental data analytics.
- The project was recognized for its outstanding corporate social responsibility initiative with an Excellence Award from the Asian CSR Awards.

Flood Simulation | Flood Prediction | Real-time Flood Maps | HPC

Honors and awards

2023 Huawei President Award for Project Management
2022 Huawei Hertz Team Award
2021 Huawei Future Star Award
2021 Huawei Timely Award
2021 Huawei Outstanding Mentor Award
2020 Huawei President Award
2020 Huawei Ascend Excellence Award
2020 Huawei Excellent Evangelist Award
2020 Huawei Future Star Award
2019 Huawei Science and Technology Diplomacy Award
2019 Huawei Handshake Award
2015 Huawei Rising Star Award
2010 Excellence Award of the Asian CSR Awards
2010 IBM First Patent Application Invention Achievement Award
2009 IBM Equity Award
2006 IBM Bravo! Award
2005 IBM Author Recognition Award
2004 Award of the Philipp-Matthaeus-Hahn Donation

Skills

Programming Languages	C, C++, Java, Forth, Javascript, CSS, XML, XSLT, Ruby, Python, Perl
AI Frameworks	TensorFlow, PyTorch, Low-Power Deep Neural Network (LPDNN), Huawei Compute Architecture for Neural Networks (CANN)
Miscellaneous Frameworks	MPI, Cuda, Hadoop, PROOF | ROOT, Linux Device Driver
Databases	MySQL, SQLite, SAP HANA, MySQL, Oracle Database
Development Tools	Make, Configure, GNU toolchain, Ant, SVN, git
Middleware	GPFS, Open Fabrics RDMA Stacks
Operating Systems	Mac OS X, Windows Server, Windows 7, Linux Redhat, Linux CentOS
Others	UML

Languages skills

German	●●●●●
English	●●●●●
French	●○○○○

Strengths

- Immerse in different cultures
- Understand the people around me
- Promote an environment of trust, diversity, and open-mindedness

Publications

2013 El Sayed, S., Graf, S., Hennecke, M., Pleiter, D., Schwarz, G., Schick, H., & Stephan, M. **Using GPFS to manage NVRAM-based storage cache**. Lecture Notes in Computer Science (Including Subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 7905 LNCS, 435–446.
https://doi.org/10.1007/978-3-642-38750-0_33

2010 Baier, H., Boettiger, H., Drochner, M., Eicker, N., Fischer, U., Fodor, Z., … Winter, F. **QPACE: Power-efficient parallel architecture based on IBM PowerXCell 8i**. Computer Science - Research and Development, 25(3–4), 149–154.
https://doi.org/10.1007/s00450-010-0122-4

2010 Strunk, J., Hiltscher, J., Rehm, W., & Schick, H. **Communication architectures for run-time reconfigurable modules in a 2-D mesh on FPGAs**. Proceedings - 2010 International Conference on Reconfigurable Computing and FPGAs, ReConFig 2010, 49–54.
https://doi.org/10.1109/ReConFig.2010.33

2009 Strunk, J., Heinig, A., Volkmer, T., Rehm, W., & Schick, H. J. **Run-Time Reconfiguration for HyperTransport Coupled FPGAs using ACCFS**. First International Workshop on HyperTransport Research and Applications.

2009 Strunk, J., Volkmer, T., Stephan, K., Rehm, W., & Schickz, H. **Impact of run-time reconfiguration on design and speed - A case study based on a grid of run-time reconfigurable modules inside a FPGA**. IPDPS 2009 - Proceedings of the 2009 IEEE International Parallel and Distributed Processing Symposium.
https://doi.org/10.1109/IPDPS.2009.5161221

2009 Schick, H. J. **directCell: The Cell/B.E. as a Tightly Coupled Accelerator**. International Supercomputing Conference.

2009 Penner, H., Bacher, U., Kunigk, J., Rund, C., & Schick, H. J. **DirectCell: Hybrid systems with tightly coupled accelerators**. IBM Journal of Research and Development, 53(5).
https://doi.org/10.1147/JRD.2009.5429068

2009 Strunk, J., Volkmer, T., Rehm, W., & Schick, H. **Design and performance of a grid of asynchronously clocked run-time reconfigurable modules on a FPGA**. ReConFig'09 - 2009 International Conference on ReConFigurable Computing and FPGAs, 392–397.
https://doi.org/10.1109/ReConFig.2009.24

2009 Schick, H. J. Communication Networks Attached to the IBM PowerXCell 8i I/O Fabrics. Workshop for Network Specification and Software Data Structures for the eQPACE Architecture.

2009 Schick, H. J. **Cell/B.E. tightly coupled via PCI Express. Workshop about Future Activities on High Performance Computing.**

2009 Strunk, J., Volkmer, T., Rehm, W., & Schick, H. **An on chip network inside a FPGA for run-time reconfigurable low latency grid communication**. 12th Euromicro Conference on Digital System Design: Architectures, Methods and Tools, DSD 2009, 539–546.
https://doi.org/10.1109/DSD.2009.133

2009 Heinig, A., Strunk, J., Rehm, W., & Schick, H. **ACCFS - operating system integration of computational accelerators using a VFS approach**. Lecture Notes in Computer Science (Including Subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 5453, 374–379.
https://doi.org/10.1007/978-3-642-00641-8_44

2009 Baier, H., Boettiger, H., Drochner, M., Eicker, N., Fischer, U., Fodor, Z., … Winter, F. **QPACE – a QCD parallel computer based on Cell processors**. Proceedings of Science.
http://arxiv.org/abs/0911.2174

2008 Baier, H., Boettiger, H., Drochner, M., Eicker, N., Fischer, U., Fodor, Z., … Winter, F. **Status of the QPACE Project**. XXVI International Symposium on Lattice Field Theory.
http://arxiv.org/abs/0810.1559

2008 Schick, H. J., Fischer, U., Pleiter, D., Wettig, T., & Lippert, T. **QPACE: QCD Parallel Computing on Cell/BE**. International Conference for High Performance Computing, Networking, Storage and Analysis.
http://sc08.supercomputing.org/scyourway/conference/view/post129.html

2008 Heinig, A., Strunk, J., Oertel, R., Rehm, W., & Schick, H. J. **Generalizing the SPUFS concept - A Case Study towards a Common Accelerator Interface**. Many-Core and Reconfigurable Supercomputing Conference.

2008 Heinig, A., Rehm, W., & Schick, H. J. **ACCFS (Accelerator File System) - A Case Study Towards a Generalized Accelerator Interface**. International Supercomputing Conference.

2008 Goldrian, G., Huth, T., Krill, B., Lauritsen, J., Schick, H., Ouda, I., … Fodor, Z. **QPACE: Quantum Chromodynamics Parallel Computing on the Cell Broadband Engine**. Computing in Science and Engineering.

2008 Schick, H. J., Penner, H., Hering, H., & Wohlmuth, O. **Cell/B.E. Accelerator Concept**. IBM Technical Leadership Exchange Conference.

2007 Schick, H. J., Penner, H., & Wohlmuth, O. **Slimline Open Firmware**. Power Architecture Developer Conference.

2007 Detert, U., Thomasch, A., Eicker, N., & Broughton, J. **JULI Project-Final Report**.

2007 Strunk, J., Heinig, A., Rehm, W., & Schick, H. J. **Heterogeneous Multiprocessing - On a Tightly Coupled Opteron Cell Evaluation Platform**. IBM CAS Software and Systems Engineering Symposium.

2007 Schneider, T., Wunderlich, S., Rehm, W., Hoefler, T., & Schick, H. J. **Code Optimization for Cell/B.E. - Opportunities for ABINIT - A Software Package for Physicist**. IBM CAS Software and Systems Engineering Symposium.

2007 Penner, H., Schick, H. J., Wohlmuth, O., & Hering, H. **CELL/B.E. Accelerator Concept.** IBM Early Career Conference.

2007 Schick, H. J., & Kunigk, J. **An Open Firmware**. IBM Academy of Technology Conference.

2005 Wohlmuth, O., Penner, H., Schick, H. J., Boessenkool, S., & Koch, S. **Slimline Open Firmware**. Power.Org Event in Barcelona.

2005 Schick, H. J. **Concept, Design and Implementation of a Slimline Boot Firmware for Linux on Power Architecture**. Diploma Thesis.

Lectures and talks

2023 **The Future of Computing — Navigating transformation, technology, and the balance between humans and machines**, CIO Digital Summit Europe.

2023 **Huawei Ascend AI architecture and acceleration for sparse matrix-matrix multiplication**, 4th Workshop on Embedded Machine Learning (WEML2023)

2022 **Herausforderungen und Chancen, die sich aus der Konvergenz von Big Data, High-Performance Computing und künstlicher Intelligenz ergeben**, Association of German Engineers.

2022 **Graph Neural Networks**, HPC-AI Advisory Council, Switzerland.

2021 **AI-enabled science — Challenges and opportunities arising from the convergence of artificial intelligence, high-performance computing and big data**, Industrial Talk, Software Applications with AI, Friedrich-Alexander-Universität Erlangen-Nürnberg

2020 **Huawei empowers healthcare industry with artificial intelligence technologies**, Emerging Technologies in Medicine

2019 **The Smarter Car for Autonomous Driving**, GSA European Executive Forum

2019 **Challenges of Autonomous Driving**, Association of German Engineers.

2018 **From edge computing to in-car computing**, Elektrobit Innovation Day.

2017 **Panel Discussion: Super-Computing versus Quantum Computing**, golemconference - Dawn of the Quantum Era.

2016 **Future of Hardware Architectures – Do we need new System Concepts for Artificial Intelligence?**, TNG Big Techday.

2011 **Petascale Analytics**, STRONGnet 2011 at the European Centre for Theoretical Studies in Nuclear Physics.

2011 **High Performance Computing**, Guest Colloquium for the Research Training Group LORENTZ FORCE, Lorentz Force Velocimetry and Lorentz Force Eddy Current Testing at the University of Ilmenau.

2011 **IBM Corporate Service Corps: Helping Create Interactive Flood Maps**, Association of German Engineers.

2011 **Experiences in Application Specific Supercomputer Design: Reasons, Challenges and Lessons Learned**, PRACE/LinkSCEEM-2 2011 Winter School in Nicosia.

2009 **Research Project QPACE – QCD Parallel Computing on the Cell Broadband Engine**, Association of German Engineers.

2005 **High Performance Computing: Blue Gene/L**, Association of German Engineers.

2004 **The IBM Cell Processor - Computing of tomorrow or yesterday?**, Association of German Engineers

Patents

2010 PCI Express multiplier device, computer system, method for operating PCI Express devices in a computer system, computer program product, and data processing program for operating PCI Express devices in a computer system.

2008 Apparatus for analyzing communication between a blade server and its expansion units or daughter cards.

Projects

StairwAI
2021 - 2023

https://www.ai4europe.eu/ai-community/projects/stairwai

The StairwAI project is designed to offer a matchmaking service for users of the AI-on-Demand platform. It primarily aims to assist low-tech small and medium enterprises (SMEs) in effortlessly locating AI assets, industry experts, knowledge sources, hardware resource providers, and more, thereby making AI integration more accessible and streamlined.

Artificial Intelligence | Horizon 2020 | AI Frameworks

Open Edge and HPC Innitiative
SINCE 2019

https://www.open-edge-hpc-initiative.org/

The mission of the Open Edge and HPC Initiative is to encourage the growth of an open, feature-rich ecosystem for Arm-based technologies that can support the evolving digital transformation needs across various industries. This ecosystem aims to complement and enrich existing systems, not replace them, and is open to all relevant contributors, including Independent Software Vendors (ISVs), solution providers, as well as key solution customers.

HPC

Modular Microserver DataCentre (M2DC)
2016 - 2019

https://www.m2dc.eu/

The Modular Microserver DataCentre (M2DC) project aimed to develop a modular, cost-optimized server architecture using heterogeneous microserver resources. This adaptable architecture supported a broad range of applications from image processing to cloud computing and high-performance computing, with easy integration and advanced runtime management capabilities. The result was cost-efficient appliances capable of seamless deployment in real data centre environments to run live applications.

System Architecture | Horizon 2020

Blue Gene Active Storage
2011 - 2013

https://www.slideshare.net/schihei/blue-gene-active-storage

Blue Gene Active Storage (BGAS) is a cutting-edge model for embedded parallel processing storage, designed to address the data intensive challenges prevalent at the exascale level. BGAS targets future-proof, scalable system-on-a-chip architectures and storage class memory innovations, with its efficacy already proven in current parallel systems. With its ability to seamlessly accelerate host workloads through close integration at middleware data/storage intersections, BGAS can be directly utilized by data-intensive applications to enhance overall performance.

Parallel Processing | Active Storage | Data-intensive Applications

Exascale Innovation Center (EIC)
2011 - 2013

https://www.fz-juelich.de/ias/jsc/EN/Research/HPCTechnology/ExaScaleLabs/EIC/_node.html

The Exascale Innovation Center (EIC) represents a collaborative research endeavor involving the Juelich Supercomputing Centre (JSC), Forschungszentrum Juelich, and IBM. Its primary aim is to address the immense challenges and opportunities presented by exascale computing. The complexities in energy discovery, optimization, and climate prediction necessitate the need for supercomputing resources. Achieving success at the exascale level necessitates a comprehensive program that encompasses all facets from core technology through to applications and algorithms.

Exascale Computing | Supercomputer | HPC

Blue Gene/Q
2009 - 2011

https://en.wikipedia.org/wiki/IBM_Blue_Gene#Blue_Gene/Q

Blue Gene represents a pioneering IBM Research initiative dedicated to pushing the boundaries of supercomputing. This project encompasses comprehensive exploration of advanced computer architecture, the software necessary for programming and controlling massively parallel systems, and the application of computational power to promote understanding across a variety of domains. These include biological processes, hydrodynamics, quantum chemistry, quantum chromodynamics, molecular dynamics, climate modelling, and financial modelling.

Supercomputer | HPC | PCI Express

QPACE
2008 - 2009

https://en.wikipedia.org/wiki/QPACE

QPACE, a collaborative endeavor of multiple academic institutions and the IBM Research and Development Lab in Boblingen, Germany, aimed at the development of a massively parallel, scalable supercomputer for applications in lattice quantum chromodynamics (QCD). Built upon a structure resembling a three-dimensional torus, QPACE utilizes identical processing nodes powered by the IBM PowerXCell 8i processor. These nodes are interconnected tightly through an FPGA-based, application-optimized network processor attached to the IBM PowerXCell 8i processor. The university partners included the Universities of Regensburg and Wuppertal, along with research labs DESY and Juelich, and the Universities of Ferrara and Milano.

Supercomputer | HPC | Cell/B.E.

AbiCell 2006 - 2007

https://www.scribd.com/document/23345235/Code-optimization-for-Cell-B-E...
The primary objective of this project was to assess the performance capabilities of InfiniBand connected Cell clusters. This was achieved by implementing selected parallel compute kernels of Abinit – a popular open-source code utilized for ab initio electronic structure calculations. This initiative facilitated a deeper look into optimization strategies and the potential of such cluster configurations.

Parallelization | HPC | Cell/B.E.

NICOLL 2006 - 2007

https://www.scribd.com/doc/23362882/Heterogeneous-Multiprocessing-On-a-tightly-coupled...
The aim of this project was to create a prototype solution for an interface architecture ideally suited to the needs of the Cell/B.E. processor Hardware-Software (HW-SW) infrastructure in hybrid systems. When required, device virtualization techniques were utilized. The project predominantly focused on interfacing InfiniBand, exemplifying high-speed cluster interconnects technology. When it came to collective communication operations, we specifically prioritized the Message Passing Interface (MPI).

Hybrid System | Computer Architecture | Cell/B.E. | Networking | InfiniBand

eHCA InfiniBand Adapter 2004 - 2006

https://git.kernel.org/pub/scm/linux/kernel/git/stable/linux.git/tree/drivers/infiniband/hw/ehca?h=v3.16.81
The adapter in question is utilized in high-performance computing (HPC) clusters. Its device driver was developed for Linux on PPC64 and is compatible with the unified Open Fabrics Alliance's open-source software stack for InfiniBand, a leading RDMA technology. Applications can leverage the eHCA InfiniBand adapter by directly calling IB verbs or using upper-level protocols such as the Message Passing Interface (MPI), TCP/IP over InfiniBand (IPoIB), or Socket Direct Protocol (SDP). This device driver has been included in the Linux kernel since version 2.6.19.

Linux | Linux Kernel | Networking | InfiniBand

eHEA Ethernet Adapter 2004 - 2006

https://git.kernel.org/pub/scm/linux/kernel/git/stable/linux.git/tree/drivers/net/ethernet/ibm/ehea?h=v3.16.81
The network adapter, utilized in IBM POWER6-based systems, boasts a device driver that supports key network functionalities including TCP Segmentation Offload (TSO), broadcast, multicast, Virtual LAN (VLAN), and ethtool. This device driver has been an integral part of the Linux kernel since version 2.6.19.

Linux | Linux Kernel | Networking | Ethernet